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Electrical and Electronic Engineering

EE270

Digital Electronics

4-bit Bouncing Counter

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**I confirm and declare that this report and the assignment work is entirely the product of my own efforts and I have not used or presented the work of others herein.**

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# Introduction

Review what report is about. Its main points. Conclusions.

This report aims to explore the functionality of a 4-bit Bouncing Counter which has an initial output of 15 then counts from 1 to 5 and back down to 1. The 4-bit bouncing counter was implemented using 4 JK flip-flops which were tied to input signals X1 and X0 (count and reset). The output for each flip-flop represents a bit with the output for flip-flop 3, Z3, being the most significant. 11 states were defined. 1 for the initial 15 state and the rest for counting from 1 to 5 and counting down from 5 to 1. J and K values were calculating using the next state equation for a JK flip-flop.

A range of appropriate input signals were used to test the robustness of the circuit and the outputs were compared to theoretical results to confirm correct functionality of the design.

The design could be improved by defining the invalid state (X1X0 = 11) rather than using don’t care terms. This would improve the robustness of the design as an undefined invalid state would lead to random and predictable outputs.

# Specification

Testing

Testing the onedrive share ability.